Rejection under 35 U.S.C. § 102

Claims 27-44 have been rejected as being anticipated by Kato, U.S. Patent Application Publication No. 2003/0231263. Applicant respectfully disagrees that Kato discloses all of the features of independent claims 27 and 36.

Independent claim 27 recites an integrated circuit that at least partially overlaps with a driving circuit, with an adhesive layer between the integrated circuit and the driving circuit. Applicant requests reconsideration and withdrawal of this rejection at least because Kato does not describe or suggest an adhesive layer between a driving circuit and an overlapping integrated circuit. The rejection provides no indication of where such an adhesive layer is believed to be found.

The rejection indicates that circuits 402-404 are driving circuits and circuits 413-415 are integrated circuits. See, e.g., Office action of May 2, 2005 at page 3, paragraph 1 and page 4, paragraph 3. However, circuits 414 and 415 are merely representative elements of circuits 402, 403 and 404, and circuit 413 represents the pixel region 401. See Kato at paragraphs [0077-78].

Kato does not describe or suggest an adhesive layer between any of circuits 413-415. The driving circuits 415 and 414 in Kato might be said to be overlapping. However, as shown in FIG. 1B, an interlayer insulating film 417, a reflecting electrode 410 and liquid crystals 407 lie between the source signal line driver circuit 415 and the gate signal line driver circuit 414. See Kato at FIG. 1B and paragraphs [0077, 0079, 0082 and 0083]. Notably, Kato does not disclose that any of the layers 407, 410 or 417 that lie between the driver circuits 415 and 414 include an adhesive material. As such, Kato does not describe or suggest an adhesive layer between the driving circuits 415 and 414. Accordingly, Kato does not describe or suggest an integrated circuit that at least partially overlaps with a driving circuit, with an adhesive layer between the integrated circuit and the driving circuit, as recited in claim 27.

The only element of Kato that could be argued to be an adhesive layer is Kato's sealing agent 405. However, Kato's "sealing agent 405 is formed in FIG. 1B so as to surround the pixel region 401 and the gate signal line driver circuit 402 formed on the glass substrate 400, and the source signal line driver circuit 403 and the logic circuit 404 formed on the opposing substrate

406." See Kato at paragraph [0077]. Accordingly, the sealing agent 405 is not located between overlapping circuits.

For at least these reasons, applicant requests reconsideration and withdrawal of the rejection of claim 27 and its dependent claims 28-35.

Independent claim 36 recites a first integrated circuit that is at least partially overlapped with a driving circuit and a second integrated circuit that is at least partially overlapped with the first integrated circuit. Even assuming, for the sake of argument only, that Kato discloses in FIG. 1B that the circuit 415 and the circuit 414 are overlapped, in such a case there are only two circuits that are overlapped in Kato. For example, assuming, for the sake of argument only, that circuit 415 corresponds to the claimed first integrated circuit, then circuit 414 would correspond to the claimed driving circuit (because, as recited in claim 36, first integrated circuit is at least partially overlapped with a driving circuit). In such a case, however, the limitations of claim 36 are not met because Kato does not disclose a second integrated circuit that is at least partially overlapped with the circuit 415, which, in this example, corresponds to the claimed first integrated circuit. Hence, Kato does not describe or suggest a first integrated circuit that is at least partially overlapped with a driving circuit and a second integrated circuit that is at least partially overlapped with the first integrated circuit, as recited in claim 36.

For at least this reason, applicant requests reconsideration and withdrawal of the rejection of claim 36 and its dependent claims 37-44.

Conclusion

Applicant submits that all claims are allowable.

It is believed that all of the pending issues have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this reply should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this reply, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

This reply is being filed concurrently with a Request for Continued Examination and an information disclosure statement. Enclosed is a $790.00 check for the Request for Continued Examination fee. Please apply any other charges or credits to deposit account 06-1050. No extension of time fee is believed due as January 14, 2006 fell on a Saturday and January 16, 2006 was a federal holiday within the District of Columbia.

Respectfully submitted,

Date: January 17, 2006

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